

frequency points to be computed. The calculations were performed on an IBM System/370 Model 168 machine.

ACKNOWLEDGMENT

The author wishes to thank L. R. Adkins for helpful discussions and L. Gray for fabricating the experimental devices.

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Static Capacitance Calculations for a Surface Acoustic Wave Interdigital Transducer in Multilayered Media

ADRIAN VENEMA, JOZEF J. M. DEKKERS, AND R. F. HUMPHRYES

Abstract—The static capacitance of an interdigital structure in multilayered media has been calculated. Numerical results are given for a surface acoustic wave interdigital transducer on an oxidized silicon substrate with a piezoelectric overlay. The capacitance is derived in terms of the layer thicknesses for zero and infinite substrate resistivity.

SURFACE acoustic wave (SAW) generation and detection on a nonpiezoelectric substrate such as silicon necessitates a piezoelectric overlay [1]. Examples of commonly used overlay materials include cadmium sulphide and zinc oxide. If it is intended to incorporate SAW devices and electronic components monolithically on the

same silicon slice, then for compatibility with silicon planar technology the silicon must be oxidized. In fact this is an advantage because the silicon dioxide also acts as an insulator between the interdigital transducer (IDT) and the electrically conductive silicon, thus making such monolithic integration possible. On the other hand, the acoustic propagating medium is now further complicated by the additional layer.

There are four possible transducer configurations [2] for such a multilayered structure. This choice is halved when it is deemed necessary to optimize for maximum electro-mechanical coupling. The remaining two configurations require the IDT to be embedded between the thermally oxidized silicon substrate and the piezoelectric overlay. Furthermore, one of these requires a metal electrode (in the form of a platelet) to be deposited on the top of the piezoelectric overlay immediately above the IDT. The latter has advantages at low kh_2 values (k is SAW wave-number, h_2 is piezoelectric layer thickness) where under certain conditions considerable enhancement is obtainable. At higher kh_2 values the performances of the two

Manuscript received May 2, 1977; revised August 16, 1977.

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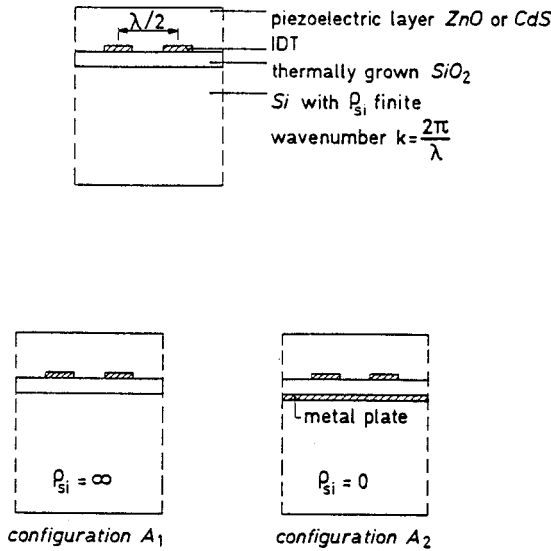


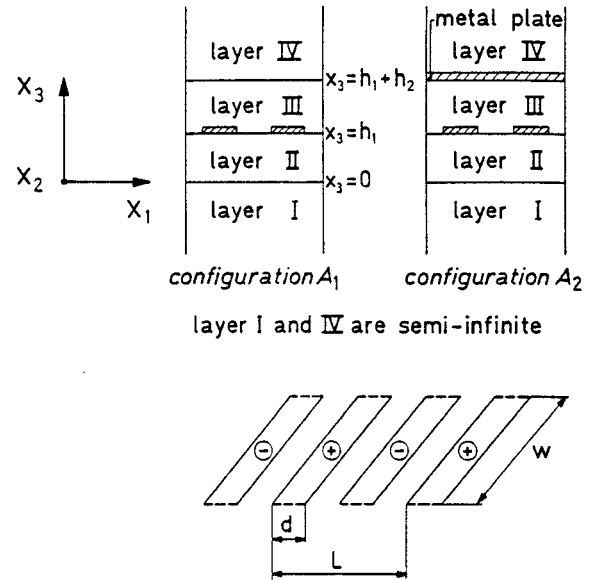
Fig. 1. Multilayered IDT structure.

configurations are practically identical. As the optimum kh_2 value for maximum electromechanical coupling exists within this region, the extra electrode is redundant. In addition, the fabrication of such an electrode is extremely difficult because of etching problems. Consequently the transducer configuration illustrated in Fig. 1 was adopted for this paper.

Several investigators [3]–[5] have solved the problem of transduction in two layered media where the substrate is nonconductive. In practical silicon devices the electrical resistivity normally ranges from 0.01 to 100 $\Omega \cdot \text{cm}$ and within this limited range it can be shown that [6], providing the value of the synchronous radian frequency is less than the silicon bulk relaxation radian frequency, then the silicon resistivity can be taken to be zero. The silicon bulk relaxation radian frequency is defined as $(\epsilon_0 \epsilon_{\text{si}} \rho_{\text{si}})^{-1}$, where ϵ_0 is the dielectric permittivity of free space, ϵ_{si} is the silicon relative dielectric permittivity, and ρ_{si} is the silicon resistivity. Above this value the resistivity can be taken to be infinite. This result is exact provided the synchronous frequency is far removed from the bulk relaxation frequency. A designer can ensure that this latter condition is satisfied by a suitable choice of substrate resistivity.

In the following an adaption of the Kino–Wagers theory [4] is developed in order to derive the static capacitance of an IDT in a multilayered structure. The assumptions used for the calculation of this capacitance for one finger pair and per unit electrode length (C_{FF}) are listed below:

- 1) the electromechanical coupling of the overlay material is weak;
- 2) the IDT has:
 - a) negligible mass loading,
 - b) electrodes with a uniformly distributed surface charge σ_s ,
 - c) electrodes with equal width-gap ratio,
 - d) unapodized electrodes;

Fig. 2. Structural identification of configuration A_1 and configuration A_2 .

- 3) the three-layer structure is unbounded in the $X_1 X_2$ plane of the substrate;
- 4) the propagating SAW is straight crested;
- 5) the piezoelectric layer material and the silicon dioxide are lossless and charge free;
- 6) the silicon substrate is charge free.

Fig. 1 illustrates the configuration of interest for a general resistivity. When the resistivity is less than $10^4 \Omega \cdot \text{cm}$ then [6] for the high-frequency approximation this degenerates into configuration A_1 of Fig. 1 and for the low-frequency approximation into configuration A_2 of Fig. 1.

A left handed Cartesian coordinate system was chosen for the configurations A_1 and A_2 . With reference to Fig. 2 each layer is labelled l and the following tensor equations hold (summation convention is applied):

$$D_{i,i}^l = 0 \quad (1)$$

$$D_i^l = \epsilon_{ij}^l E_j^l \quad (2)$$

$$E_i^l = -\phi_{,i}^l \quad (3)$$

with $l = \text{I, II, III, IV}$.

Equations (1)–(3) lead to the differential equation

$$-k^2 \epsilon_{11}^l \phi^l + \epsilon_{33}^l \phi_{,33}^l - 2jk \epsilon_{31}^l \phi_{,3}^l = 0. \quad (4)$$

The boundary conditions for configuration A_1 are

$$\lim_{x_3 \rightarrow -\infty} \phi^l = 0$$

$$\phi^{\text{I}}(0) = \phi^{\text{II}}(0)$$

$$D_3^{\text{I}}(0) = D_3^{\text{II}}(0)$$

$$\phi^{\text{II}}(h_1) = \phi^{\text{III}}(h_1) = \phi_s$$

$$D_3^{\text{III}}(h_1) - D_3^{\text{II}}(h_1) = \sigma_s$$

$$\lim_{x_3 \rightarrow +\infty} \phi^{\text{IV}} = 0 \quad (5a)$$

and for configuration A_2

$$\begin{aligned} \lim_{x_3 \rightarrow -\infty} \phi^I &= 0 \\ \phi^I(0) &= \phi^{II}(0) \\ D_3^I(0) &= D_3^{II}(0) \\ \phi^{III}(h_1 + h_2) &= 0 \\ \phi^{II}(h_1) &= \phi^{III}(h_1) = \phi_s \\ D_3^{III}(h_1) - D_3^{II}(h_1) &= \sigma_s \end{aligned} \quad (5b)$$

where D_i^I is the electric flux density, E_j^I is the electric field strength, ϕ^I is the potential which is proportional to $\exp(-jkx_1)$, ϵ_{ij}^I is the relative dielectric permittivity, and $\phi_s(k, 0) \exp(-jkx_1)$ is the potential due to the charge per unit surface area at $x_3=0$, i.e., $\sigma_s(k) \exp(-jkx_1)$.

One finger pair is assumed to be part of an infinite set of finger pairs so that $\sigma_s(k)$ becomes the Fourier component of the periodic charge distribution $\sigma(x_1)$. The capacitance per finger pair is then derived by defining $\sigma(x_1)$ (see Fig. 2) as follows:

$$\begin{aligned} \sigma(x_1) &= \frac{Q}{Wd}, \quad 0 < x_1 < d \\ \sigma(x_1) &= \frac{-Q}{Wd}, \quad \frac{1}{2}L < x_1 < \frac{1}{2}L + d \\ \sigma(x_1) &= 0, \quad \text{everywhere else in the} \\ &\quad \text{region } 0 < x_1 < L \end{aligned} \quad (6)$$

where Q is the electrode charge, d is the electrode width, L is the periodicity of the IDT, and W is the electrode aperture width.

ϕ_s is evaluated from the differential (4), upon application of the boundary conditions (5a) and (5b), which depend on the configuration under consideration, and on (6).

To determine the static capacitance the value of ϕ_s in the plane $X_3=0$ is evaluated. Configuration A_1 gives

$$\begin{aligned} \phi_s|_{x_3=0} &= \sigma_s \left[\frac{\epsilon_p^{III} |k| \{ \epsilon_p^{III} \sinh(a_3 h_2) + \epsilon_p^{IV} \cosh(a_3 h_2) \}}{\{ \epsilon_p^{III} \cosh(a_3 h_2) + \epsilon_p^{IV} \sinh(a_3 h_2) \}} \right. \\ &\quad \left. + \frac{\epsilon_p^{II} |k| \{ \epsilon_p^I \cosh(a_2 h_1) + \epsilon_p^{II} \sinh(a_2 h_1) \}}{\{ \epsilon_p^I \sinh(a_2 h_1) + \epsilon_p^{II} \cosh(a_2 h_1) \}} \right]^{-1} \end{aligned} \quad (7)$$

and for configuration A_2

$$\begin{aligned} \phi_s|_{x_3=0} &= \sigma_s \{ \epsilon_p^I + \epsilon_p^{II} \coth(a_2 h_1) \} \\ &\quad \cdot \left[|k| \{ \epsilon_p^{III} [\epsilon_p^I + \epsilon_p^{II} \coth(a_2 h_1)] \coth(a_3 h_2) \right. \\ &\quad \left. + \epsilon_p^{II} [\epsilon_p^{II} + \epsilon_p^I \coth(a_2 h_1)] \} \right]^{-1}. \end{aligned} \quad (8)$$

The capacitance C_{FF} is

$$C_{FF} = \frac{Q^2}{W \int_0^L \sigma(x_1) \phi(x_1) dx_1}. \quad (9)$$

The integral $\int_0^L \sigma(x_1) \phi(x_1) dx_1$ from this formula is equal to

$$L \sum_{-\infty}^{+\infty} \sigma_{sn}^* \phi_n$$

where

$$\sigma_{sn} = \frac{1}{L} \int_0^L \sigma(x_1) \exp(jk_n x_1) dx_1$$

in the Fourier series

$$\sigma(x_1) = \sum_{-\infty}^{+\infty} \sigma_{sn} \exp(-jk_n x_1)$$

with $k_n = 2\pi n/L$ and σ_{sn}^* is the complex conjugate of σ_{sn} .

For configuration A_1 , we then have

$$\begin{aligned} C_{FF} &= \pi \left[4 \sum_{m=0}^{\infty} \left[\frac{\sin \left\{ (2m+1) \frac{\pi d}{L} \right\}}{(2m+1) \frac{\pi d}{L}} \right]^2 \right. \\ &\quad \cdot \left[\frac{\epsilon_p^{III} (2m+1) \{ \epsilon_p^{III} \sinh(a_3^m h_2) + \epsilon_p^{IV} \cosh(a_3^m h_2) \}}{\{ \epsilon_p^{III} \cosh(a_3^m h_2) + \epsilon_p^{IV} \sinh(a_3^m h_2) \}} \right. \\ &\quad \left. \left. + \frac{\epsilon_p^{II} (2m+1) \{ \epsilon_p^I \cosh(a_2^m h_1) + \epsilon_p^{II} \sinh(a_2^m h_1) \}}{\{ \epsilon_p^I \sinh(a_2^m h_1) + \epsilon_p^{II} \cosh(a_2^m h_1) \}} \right]^{-1} \right]^{-1} \end{aligned} \quad (10)$$

and for configuration A_2

$$\begin{aligned} C_{FF} &= \pi \left[4 \sum_{m=0}^{\infty} \left[\frac{\sin \left\{ (2m+1) \frac{\pi d}{L} \right\}}{(2m+1) \frac{\pi d}{L}} \right]^2 \{ \epsilon_p^I + \epsilon_p^{II} \coth(a_2^m h_1) \} \right. \\ &\quad \cdot \left[(2m+1) \{ \epsilon_p^{III} [\epsilon_p^I + \epsilon_p^{II} \coth(a_2^m h_1)] \coth(a_3^m h_2) \right. \\ &\quad \left. \left. + \epsilon_p^{II} [\epsilon_p^{II} + \epsilon_p^I \coth(a_2^m h_1)] \} \right]^{-1} \right]^{-1} \end{aligned} \quad (11)$$

where

$$a_2^m = \frac{(2m+1)2\pi}{L} \frac{\epsilon_p^{II}}{\epsilon_{33}^{II}}$$

$$a_3^m = \frac{(2m+1)2\pi}{L} \frac{\epsilon_p^{III}}{\epsilon_{33}^{III}}$$

$$\epsilon_p^I = \{ \epsilon_{11}^I \epsilon_{33}^I - (\epsilon_{31}^I)^2 \}^{1/2}$$

$$l = \text{I, II, III, IV.}$$

In Figs. 3 and 4 the dependence of C_{FF} on the piezoelectric layer thickness and silicon conductivity is shown.

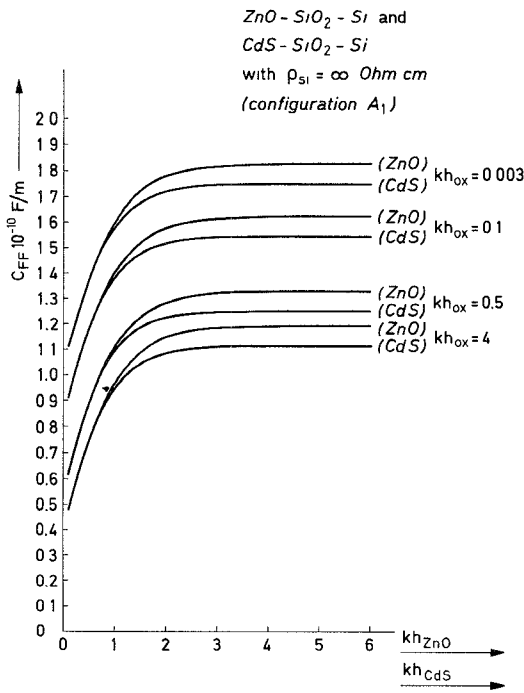


Fig. 3. The capacitance of a single finger pair as a function of kh_{ZnO} or kh_{CdS} ($h_2 \equiv h_{CdS}$ or h_{ZnO}) with kh_{ox} ($h_1 \equiv h_{ox}$) as a running parameter for the configuration A₁.

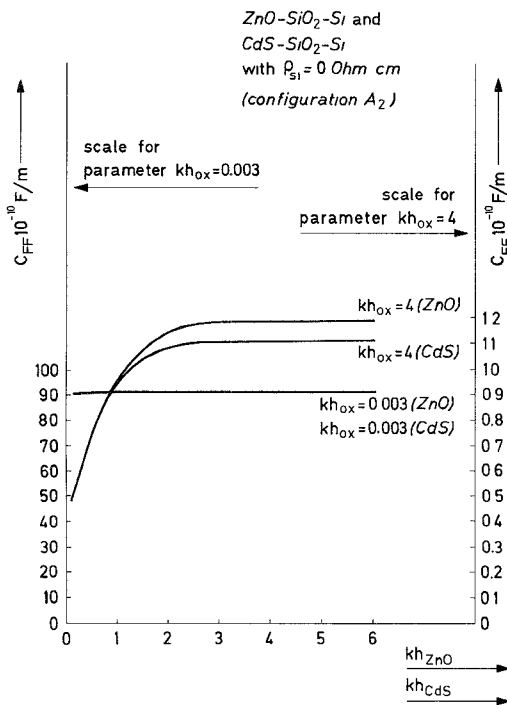


Fig. 4. The capacitance of a single finger pair as a function of kh_{ZnO} or kh_{CdS} ($h_2 \equiv h_{CdS}$ or h_{ZnO}) with the practical upper and lower limits of kh_{ox} ($h_1 \equiv h_{ox}$) as a parameter for the configuration A₂.

The piezoelectric materials are CdS and ZnO and their dielectric permittivities were obtained from Auld [8].

DISCUSSION

It is interesting to note that the Engan results [7] are obtained when, for example, $\epsilon_p^I = \epsilon_p^{II} = \epsilon_0$ in the A₁ config-

uration and $\epsilon_p^I = \epsilon_p^{II} = \epsilon_0$ in the A₂ configuration both with $kh_2 \rightarrow \infty$. Also, the calculations are in agreement with Ponamgi and Tuan [5] for $\epsilon_p^I = \epsilon_p^{II} = \epsilon_0$ in configuration A₁.

The effects of increasing kh_{ox} are easily seen from Fig. 3. Above a kh_{ox} value of 4, only minor changes occur in the IDT capacitance. Consequently, this value can be considered for design purposes as $kh_{ox} = \infty$, e.g., at $kh_{CdS} = 2.5$, $C_{FF} = 1.1034 \times 10^{-10}$ F/m for $kh_{ox} = 4$, and $C_{FF} = 1.1033 \times 10^{-10}$ F/m for $kh_{ox} = 10$. In addition, Figs. 3 and 4 show that as $kh_{CdS} \rightarrow \infty$ and $kh_{ox} \rightarrow \infty$, then $C_{FF}(A_1) = C_{FF}(A_2)$. With a zero substrate resistivity small variations in kh_{ox} for low kh_{ox} values influence the capacitance greatly.

CONCLUSIONS

1) The static capacitance of a SAW IDT is derived for multilayered media by the suitable adaption of an existing theory. The formulation was applied to a three-layer structure and numerical results given for two examples.

2) When the substrate material is silicon under certain conditions the substrate resistivity adopts a zero or infinite value. The SAW IDT is then easily modeled by application of the multilayer formulation.

3) Specifically, these conditions are: a) a silicon resistivity less than $10^4 \Omega \cdot \text{cm}$, and b) an IDT synchronous frequency less than the silicon bulk relaxation frequency.

4) Condition 3a) above is satisfied for most integrated circuit components, where the resistivities normally lie within the range 0.01 – $100 \Omega \cdot \text{cm}$.

5) The designer must choose a suitable resistivity value to satisfy condition 3b) above for his particular synchronous frequency and device application.

ACKNOWLEDGMENT

The authors are indebted to Prof. S. Middelhoek for stimulating discussions.

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